



ChEESE

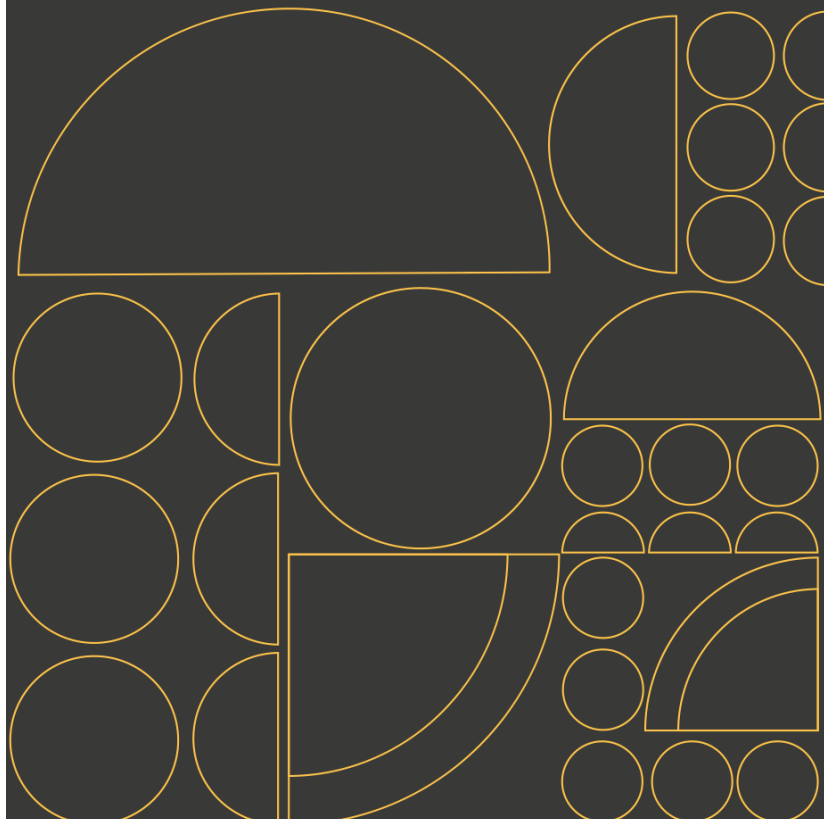
WP2 telco
February update

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WP2 team)

CINECA



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WP2: Tasks (original)

Task	Name	Lead partner	Start month	End month
2.1	Code audits	HLRS	3(27)	15(36)
2.2	Increasing the performance portability of flagship codes for different accelerators	CIN	1	48
2.3	Optimisation for Exascale	CIN	6	48
2.4	Continuous Performance Efficiency Monitoring	BSC	18	48



WP2: Tasks (updated)

Task	Name	Lead partner	Start month	End month
2.1	Code audits	HLRS	3(27)	15(30)
2.2	Increasing the performance portability of flagship codes for different accelerators	CIN	1	48
2.3	Optimisation for Exascale	CIN	6	48
2.4	Continuous Performance Efficiency Monitoring	BSC	18	48



WP2: Deliverables

D	Deliverable name	Short description	Lead	Type	Level	M
2.1	First code audit report	First code audit round results and the recommendations arising from the analysis	HLRS	R	PU	12
2.2	First report on improving code performance at exascale	Report on porting, optimization and tuning for the selected applications on the available hardware	CIN	R	PU	24
2.3	Second code audit report	Update of D2.1 and further recommendations arising from the analysis	HLRS	R	PU	30
2.4	Final report on improving code performance at exascale and Best Practice Guide	Technical report describing the achieved scalability level and related performances obtained for the selected applications on the available hardware including a final Best Practice guide	CIN	R	PU	48



WP2 (after D2.2) recap

☐ On-going tasks:

✓ **T2.1 (towards D2.3)**

✓ T2.2/T2.3 (continue the activity started in D2.2 and support Exascale ambition – best effort)

✓ **T2.4**

☐ **Commitment: reinforce a “Code-Centric” vision in ChEES-2P (flowing from WP2 to the other WPs)**

☐ **Strong commitment: internal and external dissemination of WP2 outcomes**

WP2 and WP3 (recap)

- WP2
 - full code, investigation (including porting, tuning) on CPU and GPU side. EuroHPC targeted. Code audit (but not only) driven.
 - + Performance (POP) metrics
 - + Performance Portability study on GPU for mini-apps on EuroHPC (and SDV)
- WP3
 - mini-apps investigation/co-design (including porting, tuning) on CPU and GPU side. EUPEX/EUPILOT proxies.
 - + Performance/energy efficiency metrics



WP2			
Application	Target	Task	Methodology
Full code	EuroHPC CPU & GPU	Porting Optimization for exascale Continuous performance efficiency monitoring	Code audit driven (not only) Performance POP metrics
Mini-apps	EuroHPC GPU & SDV (GPU)	Porting Optimization	Performance portability



WP3			
Application	Target	Task	Methodology
Mini-apps	- OpenSequana prototype: EUPEX (ARM+HBM & GPU) - RISC-V prototypes: EPI & EUPILOT	Porting Performance study Optimization (Scalability & Energy consumption analysis)	Co-design between SE community and Hw, Sw and Technology providers



WP2 and WP4

- WP2
 - Outcomes from T2.1/T2.3 (optimized codes, new code versions on top of different CPU/GPU flavours, ...)
 - Outcomes from T2.4 (TALP): development of new features/improvement of the tool and integration with codes.
- WP4
 - CI/CD activities.



WP2 and WP6

- WP2
 - Outcomes from T2.1/T2.3 (optimized codes, new code versions on top of different CPU/GPU flavours,...)
- WP6
 - production activities, UC, on EuroHPC hardware
 - CINECA aim to support all of the above on CINECA hardware (Leonardo.....).



WP2: publication “roadmap” (recap)

- ❑ ChEESE recommend circulating all candidate publications among partners for approval at least 30 days before the publication date.
- ❑ At a minimum, please share the title, authors, and, if possible, the abstract.
- ❑ We suggest using the cheese-science@geo3bcn.csic.es mailing list, which includes all researchers. Alternatively, you can share it through the mailing list of the relevant WPs.
- ❑ **It’s strongly suggested to acknowledge project and (eventually) WPs participants in the publication...**

T2.2/T2.3 update

