



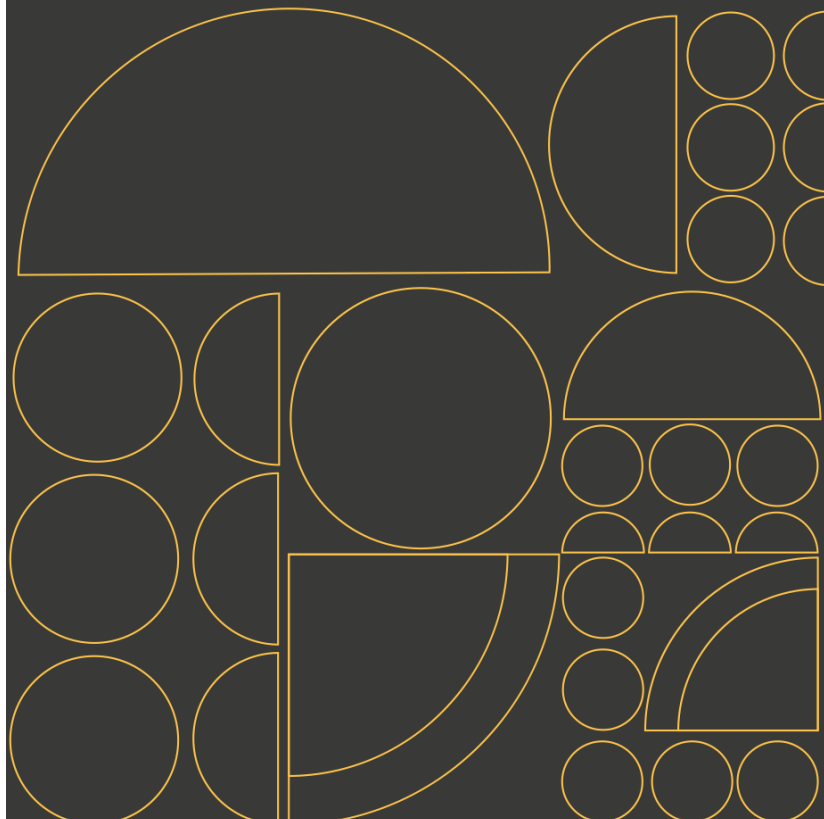
ChEESE

Work Package 2: Exascale technical challenges in flagship codes

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CINECA



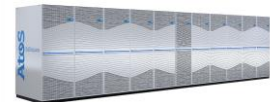
Project funded by EuroHPC under the grant agreement No 101093038.



Bridging the gap between ChEESE-2P Flagship codes and the European HPC ecosystem

Area	No	Code	Lead	ChEESE-1P	Accelerated	Mini-app
CS	1	SeisSol	LMU	yes	yes	yes
	2	SPECFEM3D	CNRS	yes	yes	yes
	3	ExaHyPE	TUM	yes	yes	no
	4	Tandem	LMU	no	no	yes
MHD	5	xSHELLS	CNRS	yes	yes	yes
T	6	HySEA	UMA	yes	yes	yes
V	7	FALL3D	CSIC	yes	yes	yes
	8	OpenPDAC	INGV	no	no	no
GD	9	LaMEM	UM	no	no	no
	10	pTatin3D	SU	no	yes	yes
GL	11	Elmer/ICE	CSC	no	no	no

Tier-0 (pre-exascale)			TOP500
LUMI	Finland	~500 PFlop/s peak	5
Leonardo	Italy	~300 PFlop/s peak	6
MN5 ACC	Spain	~250 PFlop/s peak	8



More than 1000 PFlop/s peak aggregated computing power...

...but with a variety of different (accelerated) architectures





WP2: Objectives

- | | |
|---|---|
| 1 | Address technical challenges (potentially at exascale) in the 11 flagship codes. |
| 2 | Exploit actual accelerators , in particular those targeting EuroHPC pre-exascale machines. |
| 3 | Continuously monitor the code performance efficiency during the project. |
| 4 | Produce the 4 deliverables detailed. |

WP2: Tasks

WP2 tasks					
Task	Name	Lead partner	Start month	End month	Percentage at M12 (%)
2.1	Code audits	HLRS			
2.2	Increasing the performance portability of flagship codes for different accelerators	CIN	1	48	
2.3	Optimisation for Exascale	CIN	6	48	
2.4	Continuous Performance Efficiency Monitoring	BSC	18	48	

WP2 methodology I

M12

Task 2.4

Continuous Performance Efficiency Monitoring

*First
code-audit
report*

D2.1



Task 2.1

*First report
on improving
code
performance
at exascale*

D2.2



Task 2.2

Task 2.3

*Second
code-audit
report*

D2.3



Task 2.1

*Final report
on improving
code
performance
at exascale
and Best
Practice
Guide*

D2.4



Task 2.2

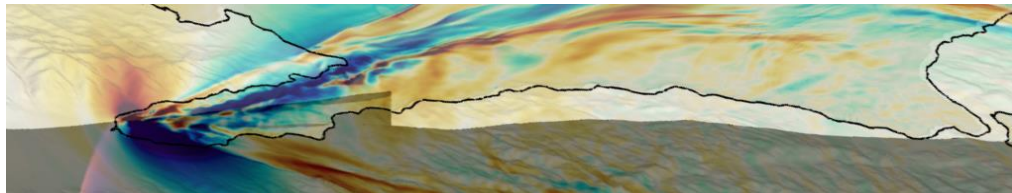
Task 2.3



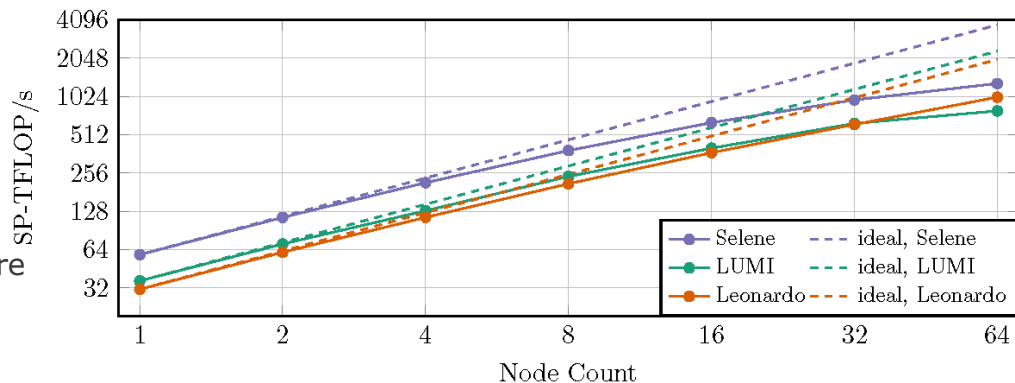
T2.1. Code audits

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T2.1. Code audits: SeisSol



- ❑ Earthquake simulation: dynamic rupture + wave propagation
- ❑ GPU porting includes elastic/acoustic/elastoplastic material (viscoelastic and poroelastic planned) and dynamic rupture
- ❑ Scalability evaluated on Leonardo, LUMI and Selene among the others:



SeisSol has been ported and optimized for GPU architectures (using primarily SYCL and CUDA as GPU programming model). SeisSol relies on CUDA graphs to mitigate the overhead for launching many kernels to GPUs. It uses a separate communication thread to ensure MPI progress for overlapping computation and communication

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T2.1. Code audits: SPECSEM3D

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T2.1. Code audits: ExaHyPE

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T2.1. Code audits: Tandem

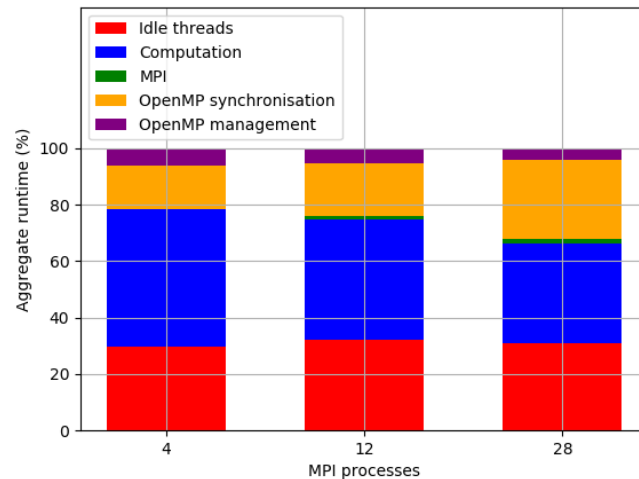
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Code Audit Table I

Flagship code	Audited version	Code Audit highlight	ChEE SE-2P Partner	EuroHPC machine used
SeisSol	MPI+SYCL+ CUDA	Code audit limited due to lack of Extrae support. Basic metrics extracted via in-built reporting functionality. Concerns in computational scalability at 64 nodes.	LMU	Leonardo booster
SPECFEM3D	MPI+CUDA		CNRS	Leonardo booster
ExaHyPE	MPI+Open MP target		TUM	Leonardo booster
Tandem	MPI		LMU	LUMI-C

• Scorep and extrae analysis

- A
- B
- C



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T2.1. Code audits: xSHELLS

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T2.1. Code audits: HySEA

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T2.1. Code audits: FALL3D

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T2.1. Code audits: OpenPDAC

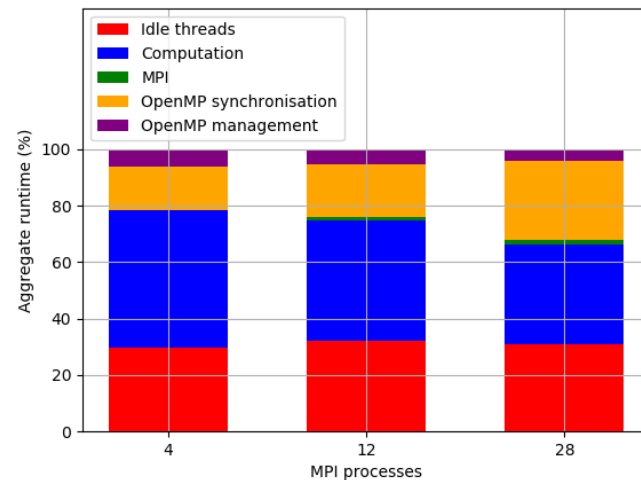
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Code Audit Table II

Flagship code	Audited version	Code Audit highlight	ChEESE -2P Partner	EuroHPC machine used
xSHELLS	MPI+CUDA	N.A.	CNRS	Vega-G
HySEA	MPI+CUDA		UMA	Leonardo booster
FALL3D	MPI+OpenACC		CSIC	Leonardo booster
OpenPDAC	MPI		INGV	LUMI-C

- Scorep and extrae analysis

- A
- B
- C



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T2.1. Code audits: LaMEM

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T2.1. Code audits: pTatin3D

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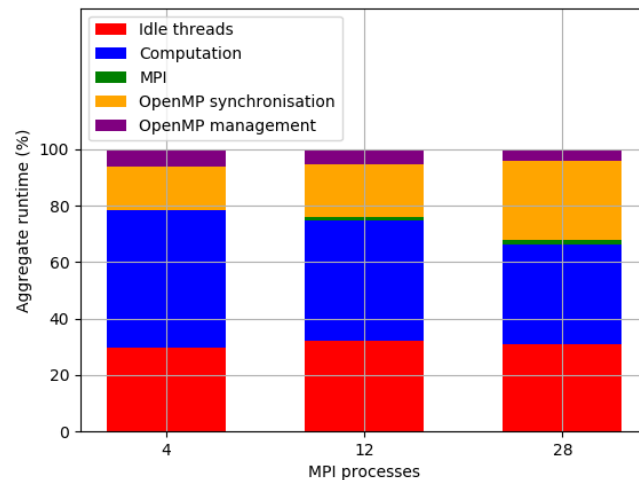
T2.1. Code audits: Elmer/ICE

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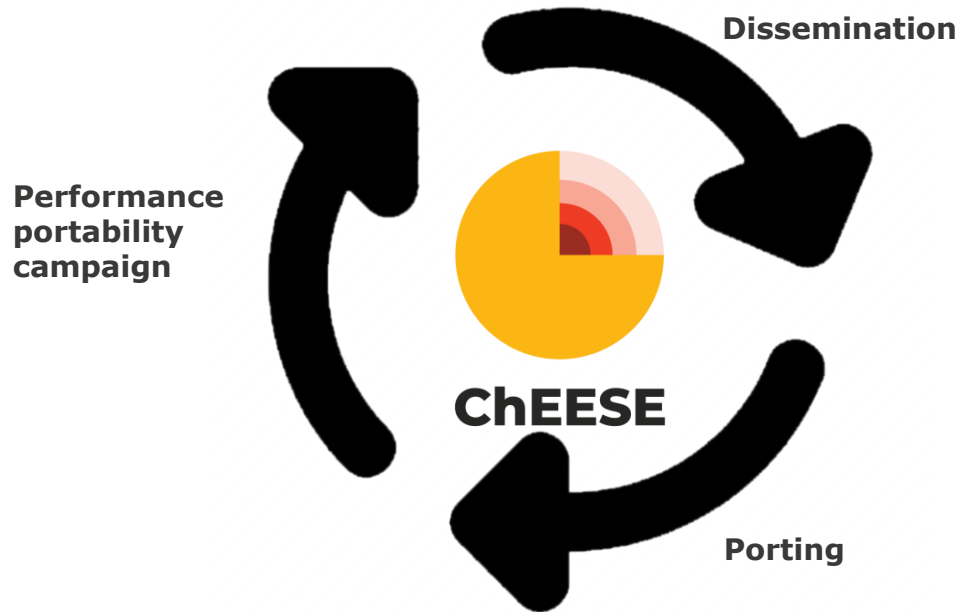
Code Audit Table III

Flagship code	Audited version	Code Audit highlight	ChEESE -2P Partner	EuroHPC machine used
LaMEM	MPI		UM	LUMI-C
pTatin3D	MPI+HIP		CNRS	LUMI-G
ELMER/ICE	MPI		CSC	LUMI-C

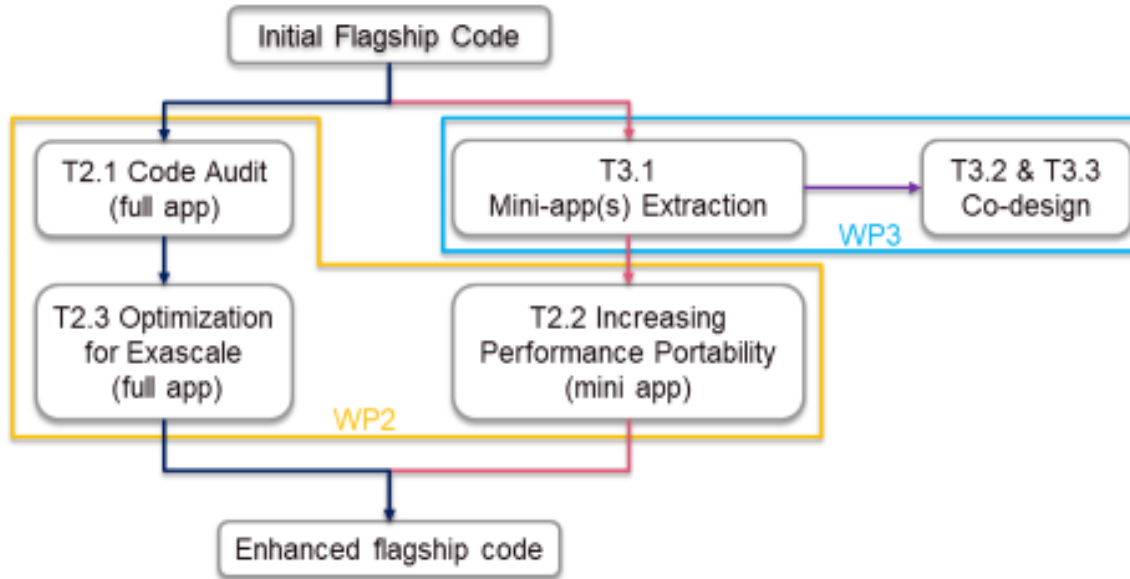
- Scorep and extrae analysis
- A
- B
- C



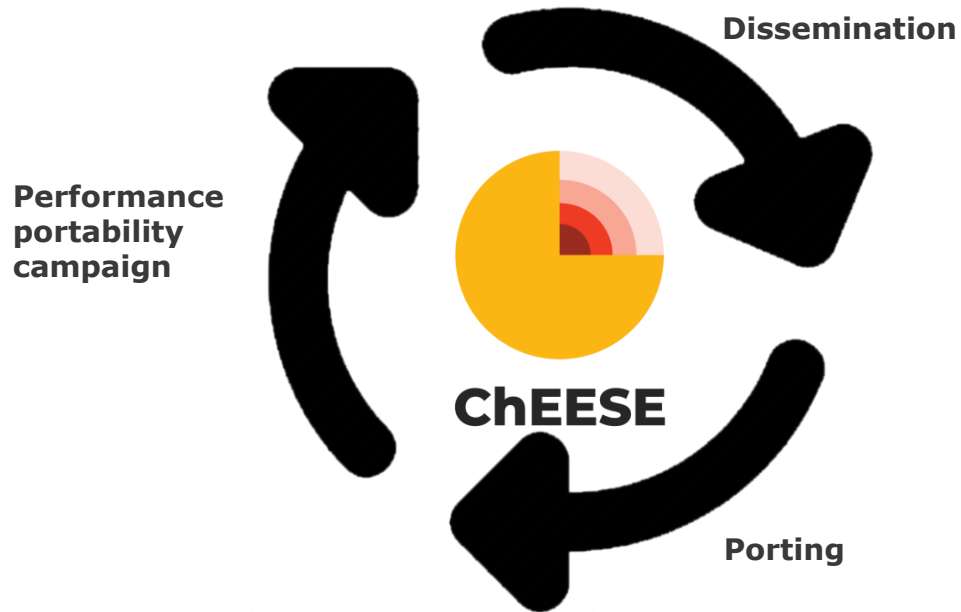
T2.2 Increasing the performance portability of flagship codes for different accelerators: the methodology



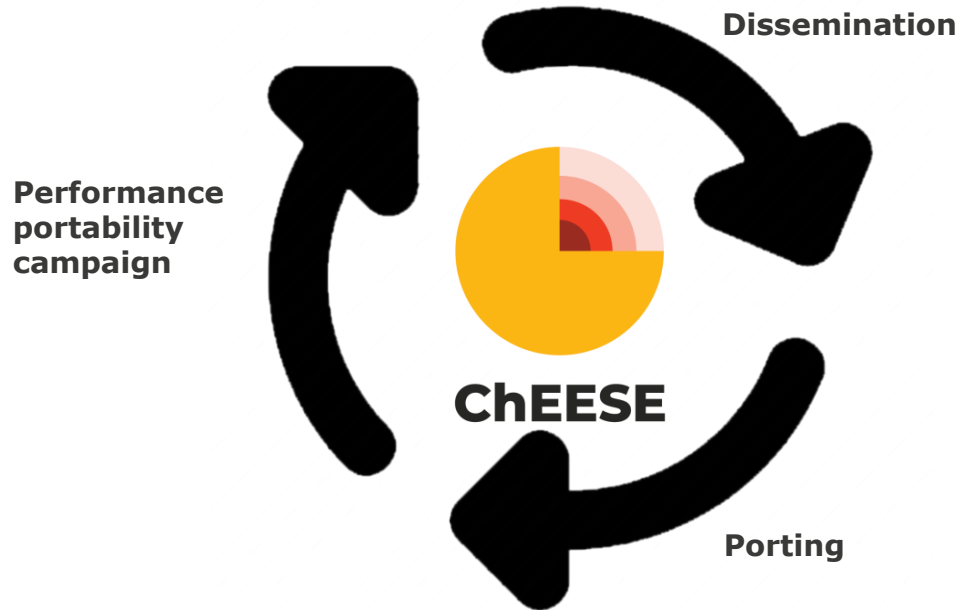
T2.2 Increasing the performance portability of flagship codes for different accelerators: the methodology: the role of mini-apps



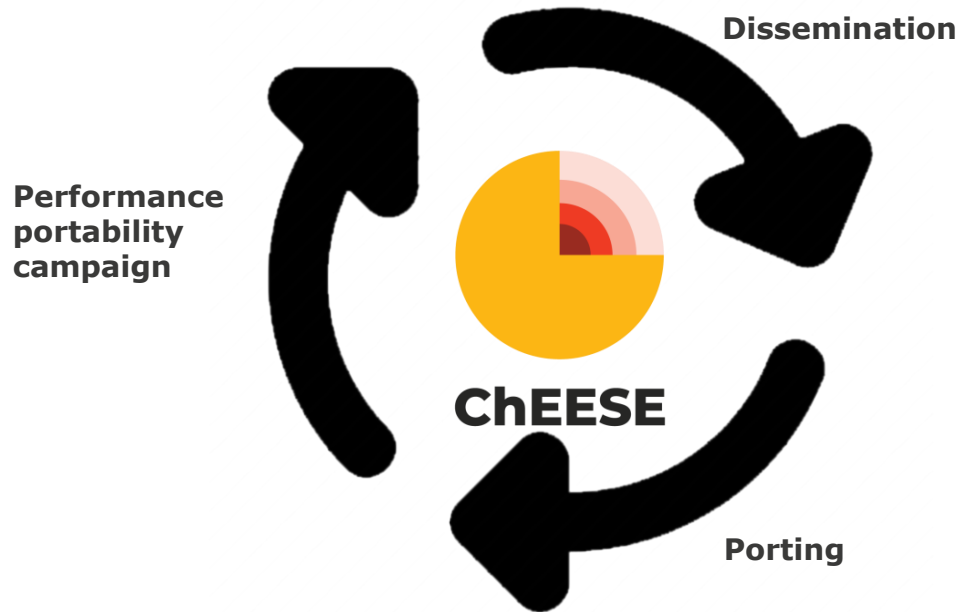
T2.2 Increasing the performance portability of flagship codes for different accelerators: dissemination



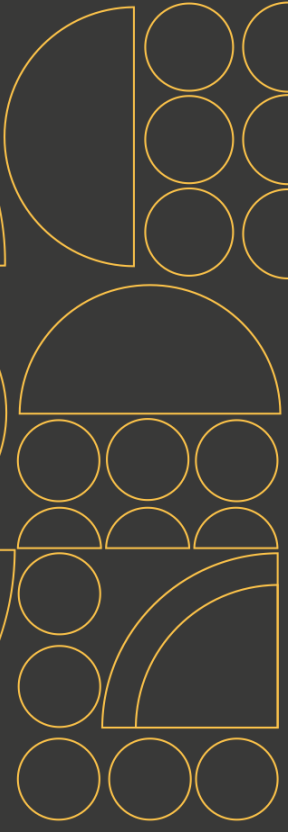
T2.2 Increasing the performance portability of flagship codes for different accelerators: porting



T2.2 Increasing the performance portability of flagship codes for different accelerators: performance portability campaign



T2.3. Optimisation for Exascale



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T2.4. Continuous Performance Efficiency Monitoring

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Other things to add · NO MANDATORY

Feel free to include two or three additional slides if necessary. For instance:

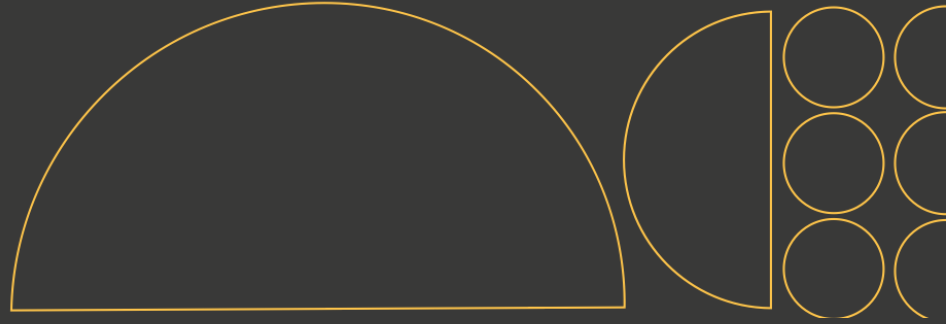
Partner Contributions

Collaborative Efforts with Others

WP2: Deliverables

D	Deliverable name	Short description	Lead	Type	Level	M
2.1	First code audit report	First code audit round results and the recommendations arising from the analysis	CIN	R	PU	18
2.2	First report on improving code performance at exascale	Report on porting, optimization and tuning for the selected applications on the available hardware	BA	R	PU	42
2.3	Second code audit report	Update of D2.1 and further recommendations arising from the analysis	HLRS	R	PU	36
2.4	Final report on improving code performance at exascale and Best Practice Guide	Technical report describing the achieved scalability level and related performances obtained for the selected applications on the available hardware including a final Best Practice guide	CIN	R	PU	48

Thank you!



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